JEDEC
STANDARD

DDR5 DIMM Labels

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JESD401-5A

(Revision of JESD401-5, May 2022)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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DDR5 DIMM LABELS

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DDR5 DIMM Labels

(From JEDEC Board Ballot JCB-21-29, formulated under the cognizance of the JC-45 Committee on DRAM Modules, item 2268.08).

1 Scope

The following labels shall be applied to all DDR5 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggg, are to be omitted when not needed.

Hybrid modules appear to the system with a “base module type” compatible interface. For example, an NVDIMM-N may be constructed with an RDIMM-style interface or an LRDIMM-style interface. What specific functions the module provides are described in an “Hybrid Media Type” field (‘n’), essentially a functional overlay on the base module type.

Terminology:

Rank or Package Rank: Collection of SDRAMs on a DIMM sharing a common chip select or copy of a chip select. Chip selects may be sourced by the host controller or by a redriver device such as registering clock driver.

Logical Rank: 3DS stacked DDR5 SDRAMs decode which internal die is selected by decoding chip identifiers (CIDs) in the command. Each package rank, therefore, may contain multiple logical ranks per package rank, increasing module capacity.

Channel: Addresses, clocks, data and associated signals that span the width of the DIMM interface from and to the host controller.

Sub-channel: The data across the width of the DDR5 standard DIMMs is divided into two independent sub-channels, each with half the data width of the full DDR5 channel. For example, an RDIMM with 80 data bits of width is internally divided into two sub-channels of 40 bits each (32 data bits and 8 ECC bits).

Example: DDR5 MRDIMM 2Rx8

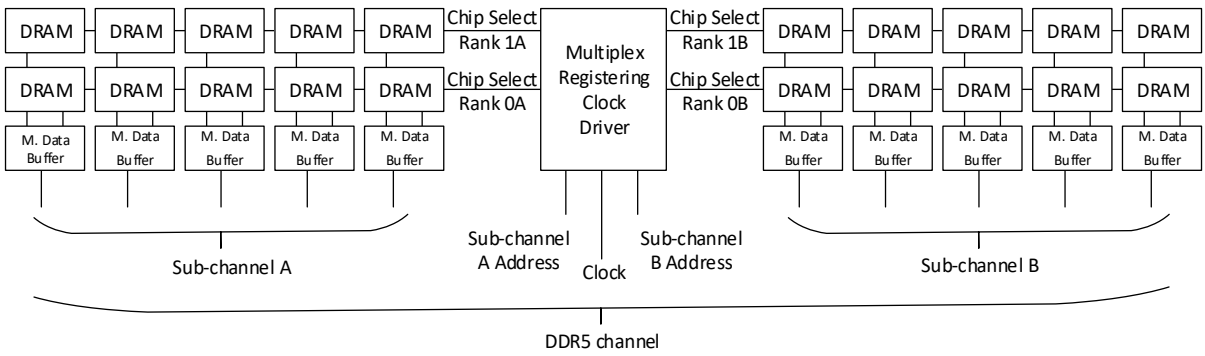

Figure 1 — Example Label

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2 DDR5 DIMM Label Format for DRAM-only Module Types Except MRDIMM

DDR5 DIMM labels for DRAM-only memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

2.1 Module Type Section

DDR5 dimm_type

Where:

dimm_type = one of:

UDIMM	EC4 UDIMM	SODIMM	EC4 SODIMM
EC4 RDIMM	EC8 RDIMM	EC8 LRDIMM	DDIMM

2.2 Technical Detail Section

ggg**GB** phee**R**x**f**f **PC5-**wwww**aa-**m**cc**d**-**bbss**-**ttt

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted). ggg**TB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)

phee**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.
p =
1 = 1 package rank of SDRAMs per sub-channel
2 = 2 package ranks of SDRAMs per sub-channel
4 = 4 package ranks of SDRAMs per sub-channel
hee =
blank = monolithic DRAM (SDP = single die package)
D2 = Dual die package (DDP)
S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank
R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

wwww = SDRAM maximum data rate in Mb/s/data pin

3200
3600
4000

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2.2 Technical Detail Section (cont'd)

4400
4800
5200
5600
6000
6400
6800
7200
7600
8000
8400
8800

aa = SDRAM speed grade
aa = Speed grade, i.e., AN, B, BN, C

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2.2 Technical Detail Section (cont'd)

Table 1 — Examples of DDR5 Monolithic or DDP Components

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63

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2.2 Technical Detail Section (cont'd)

Table 2 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63

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2.2 Technical Detail Section (cont'd)

m = Module Type
- D = Differential DIMM ("DDIMM"), with dual sub-channel with 32-bit data and 8-bit ECC per sub-channel
- E = EC4 Unbuffered DIMM ("EC4 UDIMM"), dual sub-channel with 32-bit data and 4-bit ECC per sub-channel
- L = EC8 Load Reduced DIMM ("EC8 LRDIMM"), dual sub-channel with 32-bit data and 8-bit ECC per sub-channel
- P = EC4 Registered DIMM ("EC4 RDIMM"), dual sub-channel with 32-bit data and 4-bit ECC per sub-channel
- R = EC8 Registered DIMM ("EC8 RDIMM"), dual sub-channel with 32-bit data and 8-bit ECC per sub-channel
- S = Small Outline DIMM ("SODIMM"), dual sub-channel with 32-bit data and no ECC per sub-channel
- T = EC4 Small Outline DIMM ("EC4 SODIMM"), dual sub-channel with 32-bit data and 4-bit ECC per sub-channel
- U = Unbuffered DIMM ("UDIMM"), dual sub-channel with 32-bit data and no ECC per sub-channel

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases
- Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision level used on this DIMM, Base section, SPD byte 1

ss = JEDEC SPD Revision level used on this DIMM, Module specific section, SPD byte 192

-ttt = Temperature grade (see JESD402-1 for details)
- -A1T = Operating Temperature Range A1T, -40 °C to +125 °C
- -A2T = Operating Temperature Range A2T, -40 °C to +105 °C
- -A3T = Operating Temperature Range A3T, -40 °C to +85 °C
- -ET = Operating Temperature Range ET, -25 °C to +105 °C
- -IT = Operating Temperature Range IT, -40 °C to +95 °C
- -NT = Operating Temperature Range NT, 0 °C to +85 °C
- -ST = Operating Temperature Range ST, -25 °C to +85 °C
- -RT = Operating Temperature Range RT, 0 °C to +45 °C
- -XT = Operating Temperature Range XT, 0 °C to +95 °C
- -ZZT = Vendor specific temperature range

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2.2 Technical Detail Section (cont'd)

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. The first letter in the cc field indicates which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level.

Table 3 — Pre-Production and Production DIMM Revisions

DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
Z	Z	Non-standard design

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0
ccd = F0 Production F0 module
ccd = FB Pre-production sample of raw card F1
ccd = F1 Production F1 module

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2.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> where
<vid> = DIMM Vendor ID, 4 characters (SPD bytes 512~513)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 514)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 515),
2 characters for week (SPD byte 516)
<serial> = Unique serial number assigned by manufacturer, 20 characters (SPD bytes 517~520)

(Format %02x%02x%02x%02x%02x%02x%02x%02x%02x%02x)

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2.4 Part Number Section

PN:partnumber

Where:
partnumber = module part number (SPD bytes 521~550)

2.5 Machine Readable Section

2d_barcode

Where:
2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails**(S)**serialnumber**(P)**partnumber

where technicaldetails, serialnumber, and partnumber are as defined in clauses 2.2 through 2.4 of this standard. The serialnumber field is exactly 21 characters long, including hyphens. The partnumber field come from SPD bytes 521~550.

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x), where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition; lower case characters (a-z) may be used for supplier specific information.

Delineated sections of the barcode may be in any order.

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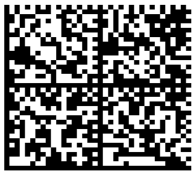
2.6 Examples



DDR5 EC8 RDIMM
64GB 2Rx4 PC5-4400B-RA2-1110-IT
SN:802C26210112345678
PN:MTA12ASF2G72PA-4H4A0

Figure 2 — Example of DDR5 EC8 RDIMM

64 GB DDR5 RDIMM (two 40 bit sub-channels with 32-bit data and 8-bit ECC per sub-channel)
2 package ranks per sub-channel
using SDP DDR5 SDRAMs
x4 data organization per SDRAM
DDR5-4400 performance, Speed grade B: CAS Latency = 36
Raw card reference design file A revision 2 used for the assembly
DDR5 base SPD revision 1.1, module SPD revision 1.0
Operating temperature IT (-40 °C to +95 °C)
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2021 week 01
Unique product serial number 12345678
Part number MTA12ASF2G72PA-4H4A0
Barcode text
(L)64GB 2Rx4 PC5-4400B-RA2-1110-IT(S)802C26160112345678(P)MTA12ASF2G72PA-4H4A0

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3 DDR5 DIMM Label Format for DRAM-only MRDIMM Module Types

DDR5 DIMM labels for DRAM-only memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

3.1 Module Type Section

DDR5 dimm_type

Where:

dimm_type = one of:

EC4 MRDIMM EC8 MRDIMM

3.2 Technical Detail Section

ggg**GB** phee**Rx**f **PC5-**yyy**/**wwaa**-**mccd**-**bbss**-**ttt

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted). ggg**TB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)

phee**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.

p =
1 = 1 package rank of SDRAMs per sub-channel
2 = 2 package ranks of SDRAMs per sub-channel
4 = 4 package ranks of SDRAMs per sub-channel

hee =
blank = monolithic DRAM (SDP = single die package)
D2 = Dual die package (DDP)
S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank

R = rank(s)

xf = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization

yyy = Module maximum data rate in 100 Mb/s/data pin (in Mux mode)
88: 8800 Mb/s/pin
96: 9600 Mb/s/pin -- reserved
104: 10400 Mb/s/pin -- reserved
112: 11200 Mb/s/pin -- reserved
120: 12000 Mb/s/pin -- reserved
128: 12800 Mb/s/pin -- reserved
136: 13600 Mb/s/pin -- reserved
144: 14400 Mb/s/pin -- reserved
152: 15200 Mb/s/pin -- reserved
160: 16000 Mb/s/pin -- reserved
168: 16800 Mb/s/pin -- reserved

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3.2 Technical Detail Section (cont'd)

176: 17600 Mb/s/pin -- reserved
ww = SDRAM maximum data rate in 100 Mb/s/data pin
32: 3200 Mb/s/pin
36: 3600 Mb/s/pin
40: 4000 Mb/s/pin
44: 4400 Mb/s/pin
48: 4800 Mb/s/pin
52: 5200 Mb/s/pin
56: 5600 Mb/s/pin
60: 6000 Mb/s/pin
64: 6400 Mb/s/pin
68: 6800 Mb/s/pin
72: 7200 Mb/s/pin
76: 7600 Mb/s/pin
80: 8000 Mb/s/pin
84: 8400 Mb/s/pin
88: 8800 Mb/s/pin
aa = SDRAM speed grade
aa = Speed grade, i.e., AN, B, BN, C

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3.2 Technical Detail Section (cont'd)

Table 4 — Examples of DDR5 Monolithic or DDP Components

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63

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3.2 Technical Detail Section (cont'd)

Table 5 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63

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3.2 Technical Detail Section (cont'd)

m = Module Type

M = EC8 Rank Multiplexed DIMM ("EC8 MRDIMM"), dual sub-channel with 32-bit data and 8-bit ECC per sub-channel

N = EC4 Rank Multiplexed DIMM ("EC4 MRDIMM"), dual sub-channel with 32-bit data and 4-bit ECC per sub-channel

cc = Reference design file used for this design (if applicable)

A = Reference design for raw card 'A' is used for this assembly

B = Reference design for raw card 'B' is used for this assembly

AC = Reference design for raw card 'AC' is used for this assembly

ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)

0~9 = Production release revisions

A~K = Pre-production releases

Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision level used on this DIMM, Base section, SPD byte 1

ss = JEDEC SPD Revision level used on this DIMM, Module specific section, SPD byte 192

-ttt = Temperature grade (see JESD402-1 for details)

-A1T = Operating Temperature Range A1T, -40 °C to +125 °C

-A2T = Operating Temperature Range A2T, -40 °C to +105 °C

-A3T = Operating Temperature Range A3T, -40 °C to +85 °C

-ET = Operating Temperature Range ET, -25 °C to +105 °C

-IT = Operating Temperature Range IT, -40 °C to +95 °C

-NT = Operating Temperature Range NT, 0 °C to +85 °C

-ST = Operating Temperature Range ST, -25 °C to +85 °C

-RT = Operating Temperature Range RT, 0 °C to +45 °C

-XT = Operating Temperature Range XT, 0 °C to +95 °C

-ZZT = Vendor specific temperature range

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3.2 Technical Detail Section (cont'd)

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. The first letter in the cc field indicates which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level.

Table 6 — Pre-Production and Production DIMM Revisions

DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
Z	Z	Non-standard design

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0
ccd = F0 Production F0 module
ccd = FB Pre-production sample of raw card F1
ccd = F1 Production F1 module

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3.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> where
<vid> = DIMM Vendor ID, 4 characters (SPD bytes 512~513)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 514)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 515),
2 characters for week (SPD byte 516)
<serial> = Unique serial number assigned by manufacturer, 20 characters (SPD bytes 517~520)

(Format %02x%02x%02x%02x%02x%02x%02x%02x%02x%02x)

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3.4 Part Number Section

PN:partnumber

Where:
partnumber = module part number (SPD bytes 521~550)

3.5 Machine Readable Section

2d_barcode

Where:
2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails**(S)**serialnumber**(P)**partnumber

where technicaldetails, serialnumber, and partnumber are as defined in clauses 2.2 through 2.4 of this standard. The serialnumber field is exactly 21 characters long, including hyphens. The partnumber field come from SPD bytes 521~550.

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x), where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition; lower case characters (a-z) may be used for supplier specific information.

Delineated sections of the barcode may be in any order.

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3.6 Examples

DDR5 EC8 MRDIMM
128GB 4D2Rx4 PC5-88/64AN-MB0-1210-XT
SN:802C26210187654321
PN:NG128DD4G2-4D4B

Figure 3 — Example of DDR5 EC8 MRDIMM

128 GB DDR5 MRDIMM (two 40 bit sub-channels with 32-bit data and 8-bit ECC per sub-channel)
4 package ranks per sub-channel
using DDP DDR5 SDRAMs
x4 data organization per SDRAM
Maximum module data rate in Mux mode is 8800 Mbps/data pin
Maximum module data rate in Rank mode is 6400 Mbps/data pin
Speed grade AN: CAS Latency = 46 at DDR5-6400 speed
Raw card reference design file B revision 0 used for the assembly
DDR5 base SPD revision 1.2, module SPD revision 1.0
Operating temperature range XT (0 °C to +95 °C)
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2021 week 01
Unique product serial number 802C26210187654321
Part number NG128DD4G2-4D4B
Barcode text
(L)128GB 4D2Rx4 PC5-88/64AN-MB0-1210-XT(S)802C26210187654321(P)NG128DD4G2-4D4B

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4 DDR5 DIMM Label Format for Hybrid Module Types

DDR5 DIMM labels for Hybrid memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label. In addition, modules with self-encryption have a section with an encryption identifier for data recovery, below the serial number section.

4.1 Module Type Section

DDR5 dimm_type

Where:

dimm_type = one of:

EC8 NVRDIMM-N EC4 NVRDIMM-N
EC8 NVLRDIMM-N EC4 NVLRDIMM-N
EC8 NVMRDIMM-N EC4 NVMRDIMM-N

4.2 Technical Detail Section

ggg**GB** phee**Rx**ff **N**nn**5-**wwwwa**-**mccd**-**bbss**-**ttt

MRDIMM-based hybrid module ONLY:

ggg**GB** phee**Rx**ff **N**nn**5-**yyy**/**wwa**-**mccd**-**bbss**-**ttt

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted). ggg**TB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)

phee**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.

p =
1 = 1 package rank of SDRAMs per sub-channel
2 = 2 package ranks of SDRAMs per sub-channel
4 = 4 package ranks of SDRAMs per sub-channel

hee =
blank = monolithic DRAM (SDP = single die package)
D2 = Dual die package (DDP)
S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

nn = Module type
N = NVDIMM-N module type

ww = SDRAM maximum data rate in 100 Mb/s/data pin
3200
3600

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4.2 Technical Detail Section (cont'd)

4000
4400
4800
5200
5600
6000
6400
6800
7200
7600
8000
8400
8800

aa = SDRAM speed grade
aa = Speed grade, i.e., AN, B, BN, C

yyy = Module maximum data rate in 100 Mb/s/data pin (operating in Mux mode)
8800
9600 -- reserved
10400 -- reserved
11200 -- reserved
12000 -- reserved
12800 -- reserved
13600 -- reserved
14400 -- reserved
15200 -- reserved
16000 -- reserved
16800 -- reserved
17600 -- reserved

Examples:

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4.2 Technical Detail Section (cont'd)

Table 7 — Examples of DDR5 Monolithic Components

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63

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4.2 Technical Detail Section (cont'd)

Table 8 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63

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4.2 Technical Detail Section (cont'd)

m = Module Type (How DIMM appears electrically to the system)
- L = Load Reduced DIMM ("LRDIMM"), dual sub-channel with 32-bit data and 8-bit ECC per sub-channel
- M = EC8 Rank Multiplexed DIMM ("EC8 MRDIMM"), dual sub-channel with 32-bit data and 8-bit ECC per sub-channel
- P = EC4 Registered DIMM ("EC4 RDIMM"), dual sub-channel with 32-bit data and 4-bit ECC per sub-channel
- R = Registered DIMM ("RDIMM"), dual sub-channel with 32-bit data and 8-bit ECC per sub-channel

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases
- Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision level used on this DIMM, Base section, SPD byte 1

ss = JEDEC SPD Revision level used on this DIMM, Module specific section, SPD byte 192

-ttt = Temperature grade (see JESD402-1 for details)
- -A1T = Operating Temperature Range A1T, -40 °C to +125 °C
- -A2T = Operating Temperature Range A2T, -40 °C to +105 °C
- -A3T = Operating Temperature Range A3T, -40 °C to +85 °C
- -ET = Operating Temperature Range ET, -25 °C to +105 °C
- -IT = Operating Temperature Range IT, -40 °C to +95 °C
- -NT = Operating Temperature Range NT, 0 °C to +85 °C
- -ST = Operating Temperature Range ST, -25 °C to +85 °C
- -RT = Operating Temperature Range RT, 0 °C to +45 °C
- -XT = Operating Temperature Range XT, 0 °C to +95 °C
- -ZZT = Vendor specific temperature range

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4.2 Technical Detail Section (cont'd)

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. The first letter in the cc field indicates which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level.

Table 9 — Pre-Production and Production DIMM Revisions

DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
Z	Z	Non-standard design

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0
ccd = F0 Production F0 module
ccd = FB Pre-production sample of raw card F1
ccd = F1 Production F1 module

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4.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> (Format %02x%02x%02x%02x%02x%02x%02x%02x%02x%02x) where
<vid> = DIMM Vendor ID, 4 characters (SPD bytes 512~513)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 514)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 515),
2 characters for week (SPD byte 516)
<serial> = Unique serial number assigned by manufacturer, 20 characters (SPD bytes 517~520)

4.4 Part Number Section

PN:partnumber

Where:

partnumber = module part number (SPD bytes 521~550)

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4.5 Physical Presence Security Identifier Section

PSID:psid

Where:
psid = Physical Presence Security ID, exactly 32 printable characters
as defined by the Trusted Computing Group Storage Opal SSC Feature Set: PSID specification; see trustedcomputinggroup.org for details

This field is required for hybrid modules that incorporate self-encryption to allow data recovery.

4.6 Machine Readable Section

2d_barcode

Where:
2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails**(S)**serialnumber**(P)**partnumber or

(L)technicaldetails**(S)**serialnumber**(P)**partnumber**(K)**psid for modules supporting self-encryption

where technicaldetails, serialnumber, partnumber, and psid are as defined in clauses 4.2 through 4.5 of this standard. The serialnumber field is exactly 21 characters long, including hyphens. The partnumber field comes from SPD bytes 521~550. The psid field, when included, is exactly 32 characters long.

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x), where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition; lower case characters (a-z) may be used for supplier specific information. Delineated sections of the barcode may be in any order.

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4.7 Examples

DDR5 EC8 NVRDIMM-N
64GB 1Rx4 NN5-4400B-RZZZ-1112-XT
SN:802C26200112345678
PN:MTA12ASF2G72PA-4H4A0
PSID:87654321876543218765432187654321

Figure 4 — Example of DDR5 EC8 NVRDIMM-N

64 GB DDR5 NVDIMM-N (dual sub-channel with 32-bit data and 8-bit ECC per sub-channel)
Appears as an RDIMM with 1 package rank per DIMM using SDP DDR5 SDRAMs with x4 data organization per SDRAM
DDR5-4400 performance, speed grade B: CAS Latency = 36
No standard raw card reference design file used for the assembly
DDR5 base SPD revision 1.1, module SPD revision 1.2
Extended operating temperature grade
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2020 week 01
Unique product serial number 12345678
Part number MTA12ASF2G72PA-4H4A0
PSID self-encryption key 87654321876543218765432187654321
Barcode text
(L)64GB 1Rx4 NN5-4400B-RZZZ-1112-XT(S)802C26160112345678(P)MTA12ASF2G72PA-4H4A0(K)87654321876543218765432187654321

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Annex A — (Informative) Differences between Document Revisions

A.1 Differences between JESD401-5A and JESD401-5

- Clause 1 (Scope): Clarified terminology, picture of example module; fixed NVDIMM section adding nn field
- Added MRDIMM, deleted NVDIMM-P
- Separated DRAM speed from module speed
- Changed wording back for wwww to SDRAM speed
- Shortened MRDIMM label length using abbreviated speeds, added EC4 MRDIMM option
- Changed references of 2:1 to Mux, 1:1 to Rank

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Standard Improvement Form **JEDEC Standard No. JESD401-5A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

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